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Dedicated to Professor M.P. Kaźmierkowski
on the occasion of his 70th birthday

A predictive estimation based control strategy for a quasi-resonant dc-link inverter

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Abstract. Control of parallel quasi resonant dc link inverters (PQRDCLI) is usually based on dc link input inverter current. Instead of a direct measurement of this noise sensitive and fast changing current signal – its estimation with one step prediction may be considered. Estimation of an input inverter current is based on inverter output current measurements, applied in most of power electronics controlled ac drives. In this paper, the PQRDCLI fed induction motor (IM) with a predictive current estimation stabilizes resonant inverter output voltage slopes du/dt independently of load. By control of output voltage derivatives, reduction of overvoltage spikes and common mode motor currents is achieved. An analysis of the PQRDCLI control with a predictive current estimation strategy is verified by the Saber system simulation and experimental tests in a laboratory setup.

Key words: resonant converters, ZVS three-phase inverter, current estimation.

1. Introduction

Resonant and quasi-resonant dc link voltage inverters (QRDCLI) for drive applications offer many interesting features, as: -zero voltage switching (ZVS) operation of main inverter switches, -limitation of voltage commutation derivatives, leading to -reduction of electromagnetic interference emissions (EMI) and -increased protection against winding insulation faults [1]. Over two-decades development of this class of inverters has given birth to original topologies with control strategies, where commutation of an inverter state is preceded by an instant when the dc link voltage is decreasing resonantly to zero [2]. In the QRDCLI an initial instant of each one resonant cycle is commanded from microcontroller [3–5]. Thus, an adoption of a pulse width or the pulse density modulation (PWM/PDM) strategies to control the output voltage amplitude and phase is possible. Moreover, by appropriate timing of QRDCLI switches, one may stabilize resonant inverter output voltage slopes du/dt independently of load conditions [6–7]. However, the QRDCLI has not become a commercial solution for ac drives control. Some of implementation obstacles are sensitive measurement of current/voltage control signals, which have to be used for high frequency, precise timing of auxiliary resonant circuit switches [8].

In this paper, instead of the direct measurement of noise sensitive and fast changing input inverter current, its estimation with one-step-prediction based on inverter output current measurements is proposed. The presented method is applied to control the parallel QRDCLI feeding an induction machine (IM), (Fig. 1). In Sec. 2, a brief analysis of the PQRDCLI operation is recalled. Then, estimation scheme using one step prediction of input inverter current with timing control of PQRDCLI switches is derived and validated by the simulation study in Sec. 3. Digital control implementation issues are briefly reported in Sec. 4. Finally, experimental results of the PQRDCLI operation obtained in a laboratory setup are presented in Sec. 5.

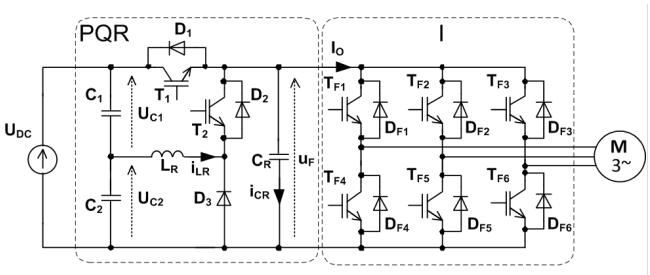

Fig. 1. Parallel quasi-resonant DC link inverter; (PQR – parallel quasi-resonant circuit, I – inverter, M – induction motor)

2. Pqrdcli operation

The full cycle analysis of the PQRDCLI is recalled from [7] in an abbreviated form. Its operation is based on the following subintervals, as depicted in Fig. 2.

Interval A. An initial steady-state, transistor T_1 is turned on conducting load current I_O, while T_2 is turned off.

Interval B. After transistor T_2 is turned on, it conducts linearly increasing inductor current i_{LR} in the circuit: C_1- T_1-T_2-L_R. That is

$$i_{LR}\,(t > t_1) = -\frac{U_{C1}}{L_R}(t - t_1). \tag{1}$$

At the end of interval, inductor current i_{LR} should reach sufficient value $I_{LR(\min)} \leq 0$ to discharge capacitor C_R with approximately constant current $-I_{CR} = (I_{LR(\min)} - I_O)$.

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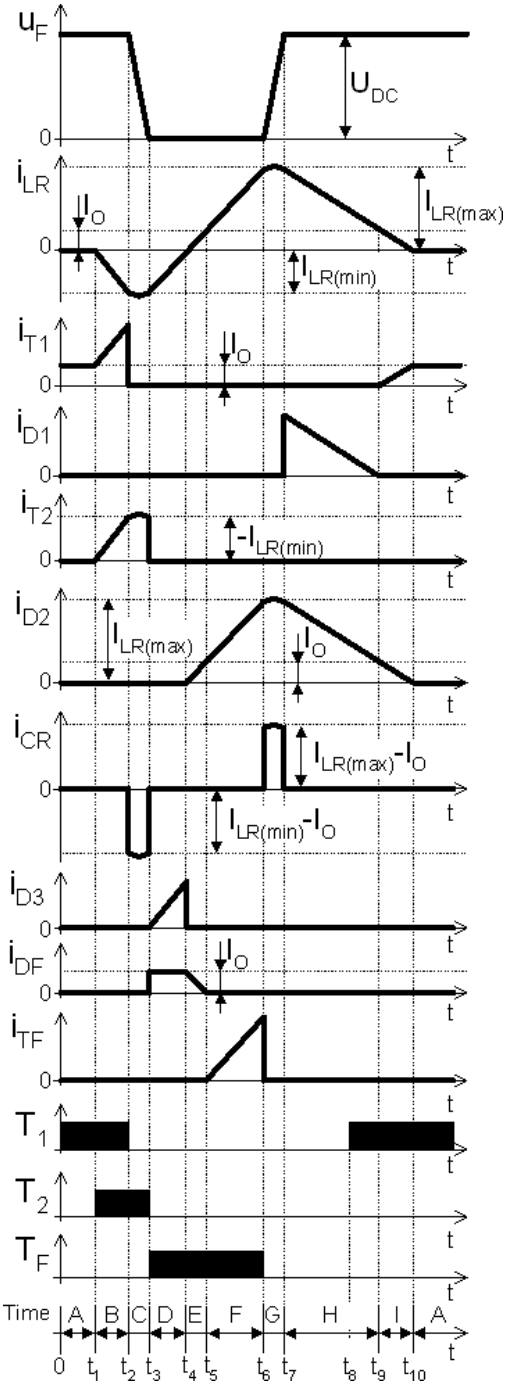

Fig. 2. Transient waveforms for the load current $I_O > 0$

Interval C. Transistor T_1 turn-off instant at the ZVS conditions initiates a resonant discharge of the capacitor C_R. Voltage u_F decreases to zero with approximately constant rate of change

$$\frac{du_F}{dt} \cong \frac{I_{LR(\min)} - I_O}{C_R}. \tag{2}$$

Interval D. At moment t_3, the capacitor voltage $u_F = 0$. Transistors of the inverter bridge (T_F) are switched on and transistor T_2 is switched off at the ZVS conditions. Inductor current i_{LR} decreases linearly

$$i_{LR}\,(t > t_3) = i_{LR}(t_3) + \frac{U_{C2}}{L_R}(t - t_3). \tag{3}$$

Interval E. At the instant t_4, positive current i_{LR} starts recharging the inductor L_R

$$i_{LR}\,(t > t_4) = \frac{U_{C2}}{L_R}(t - t_4). \tag{4}$$

Interval F. As $i_{LR} > I_O$, inverter transistors start to conduct. Inductor current i_{LR} should reach sufficient value $I_{LR(\max)}$ to charge capacitor C_R with approximately constant current $I_{CR} = (I_{LR(\max)} - I_O)$

$$i_{LR}\,(t > t_5) = I_O + \frac{U_{C2}}{L_R}(t - t_5). \tag{5}$$

Interval G. At the instant t_6, inverter transistors are set to the new state at the ZVS conditions. The capacitor voltage u_F resonant recharging is approximately linear, according to

$$\frac{du_F}{dt} \cong \frac{I_{LR(\max)} - I_O}{C_R}. \tag{6}$$

Interval H. When the capacitor voltage u_F reaches the value of the supply voltage U_{DC}, discharging inductor energy is performed. That is

$$i_{LR}\,(t > t_7) = i_{LR}(t_7) - \frac{U_{C1}}{L_R}(t - t_7). \tag{7}$$

During this interval, transistor T_1 is switched on at ZVS conditions.

Interval I. The current in T_1 starts to flow when $i_{LR} < I_O$. At this period, the inductor current i_{LR} decreases linearly to zero (7) at instant t_{10}.

In the case of negative load current I_O <0, consecutive operation intervals are the same, except that *intervals* B and F have to be adapted to a variable load current I_O, which is obtained from the estimator (Fig. 3a). In order to assure constant discharging-recharging current of the resonant capacitor I_{CR}, independently of sign and value of the load current, as it follows from Eqs. (2) and (6)

$$I_{CR} = \begin{cases} -I_{LR(\min)} + I_O & \text{discharging} \\ I_{LR(\max)} - I_O & \text{recharging} \end{cases} \tag{8}$$

evaluation of the load current I_O must be performed every cycle operation. Full cycle operation, as described above, is initiated each time before the inverter changes its state. The *interval* B is started by an interrupt signal from the modulator. The commutation between *intervals* C and D is controlled by the first comparator T_{CD} sensing the discharge of capacitor C_R (voltage below the threshold U_{F_ref}). The ZVS of transistor T_1 in the *interval* H is enabled when $u_F \geq U_{DC}$, which is detected by the second comparator T_H.

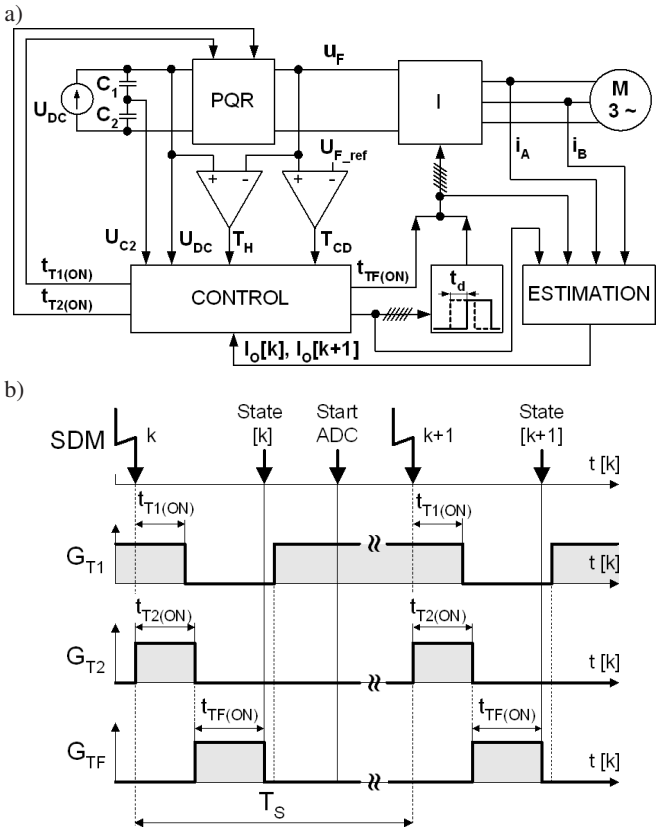

Fig. 3. Predictive estimation and control system; a) block diagram, b) cycle timing

3. Predicitive estimation and control strategy

Direct measurement of an input inverter current I_O is difficult, because of design constraints of inverter bus-bars, requiring large copper plates minimizing total stray inductance between powers modules and dc link input capacitor C_R [9]. Instead of mounting current sensor at the inverter input – an estimation scheme is proposed to measure currents at the inverter output, usually carried out in two or three phases i_A, i_B, i_C.

The two-level voltage source inverter I, depicted in Fig. 1 possesses six active switch states and two zero switch states, which can be defined by switching state of the three upper transistors $T_{F1} - T_{F2} - T_{F3}$. Simplifying inverter operation to an ideal electric switchboard, the input load current I_O is a function of the inverter states and can be determined by one of the three-phase output currents, as in Table 1.

Table 1
Estimation of the input load current $\widehat{I}_O$

T_{F1}	T_{F2}	T_{F3}	$\widehat{I}_O$
1	0	0	i_A
0	1	1	$-i_A$
0	1	0	i_B
1	0	1	$-i_B$
0	0	1	i_C
1	1	0	$-i_C$
1	1	1	0
0	0	0	0

In this study, the PQRDCLI operation cycle is controlled by the sigma-delta modulator (SDM) interrupts with constant sampling frequency T_s, shown in Fig. 3b). Start of analog to digital conversion (Start ADC) of output currents i_A, i_B and input voltages U_{C2}, U_{DC} is initiated with a delay, when the inverter state is set. Then, two estimates of input current are derived: -estimate $\widehat{I}_O(k)$ based on actual inverter state [k], and - estimate with one step prediction $\widehat{I}_O(k+1)$ for the next sampling period [k+1], when inverter will be switched to the successive new state calculated in the SDM [10–12].

From Eqs. (2) and (8), duration of the *interval B* is obtained

$$t_{T1(ON)} = t_2 - t_1 = \frac{L_R}{U_{C1}}\left(I_{CR} - \widehat{I}_O(k)\right). \tag{9}$$

In order to adapt the next time interval $t_{TF(ON)} = t_6 - t_3$ for inverter transistors turn-on, first $i_{LR}(t_3)$ has to be analyzed from resonant recharge process in the $L_R - C_R$ circuit initiated in the *interval C* by transistor T_1 turn-off. Resulting response of the inductor current i_{LR} is the following

$$\begin{aligned} i_{LR}(t > t_2) &= \left(I_{LR(\min)} - I_O\right)\cos\omega(t - t_2) \\ &-U_{C1}\sqrt{\frac{C_R}{L_R}}\sin\omega(t - t_2) + I_O, \end{aligned} \tag{10}$$

where the resonance frequency is defined as

$$\omega = 1\Big/\sqrt{L_R C_R}.$$

Substituting load current I_O by its estimate in Eqs. (8) and (10)

$$\begin{aligned} i_{LR}(t_3) &= -I_{CR}\cdot\cos\omega(t_3 - t_2) \\ &-U_{C1}\sqrt{\frac{C_R}{L_R}}\sin\omega(t_3 - t_2) + \widehat{I}_O(k), \end{aligned} \tag{11}$$

$$I_{CR} = \begin{cases} -I_{LR(\min)} + \widehat{I}_O(k) & \text{discharging} \\ I_{LR(\max)} - \widehat{I}_O(k+1) & \text{recharging} \end{cases} \tag{12}$$

Assuming capacitor current $I_{CR} = C_R du_F/dt$ as constant design parameter, from Eq. (12) results

$$I_{LR(\max)} = C_R\frac{du_F}{dt} + \widehat{I}_O(k+1). \tag{13}$$

Finally, from Eqs. (11) and (13) $t_{TF(ON)}$ is obtained

$$t_{TF(ON)} = t_6 - t_3 = \frac{L_R}{U_{C2}}\left(I_{LR(\max)} - i_{LR}(t_3)\right). \tag{14}$$

In the following simulation study carried out in the Saber/Mast program [13], the input inverter current I_O for an arbitrary operation period of the PQRDCLI has been compared: -with its estimate $\widehat{I}_O(k)$, based on an actual inverter state, and with one-step prediction estimate $\widehat{I}_O(k+1)$. SDM operated at the sampling period, $Ts = 50$ μs. Motor current measurements with analog to digital conversion and estimation procedure were completed 20 μs before the end of the sampling period Ts. Results of estimation transients, as depicted in Fig. 4, confirm coherence of the current estimate $\widehat{I}_O(k)$ and one-step prediction estimate $\widehat{I}_O(k+1)$ with the input inverter current I_O waveform.

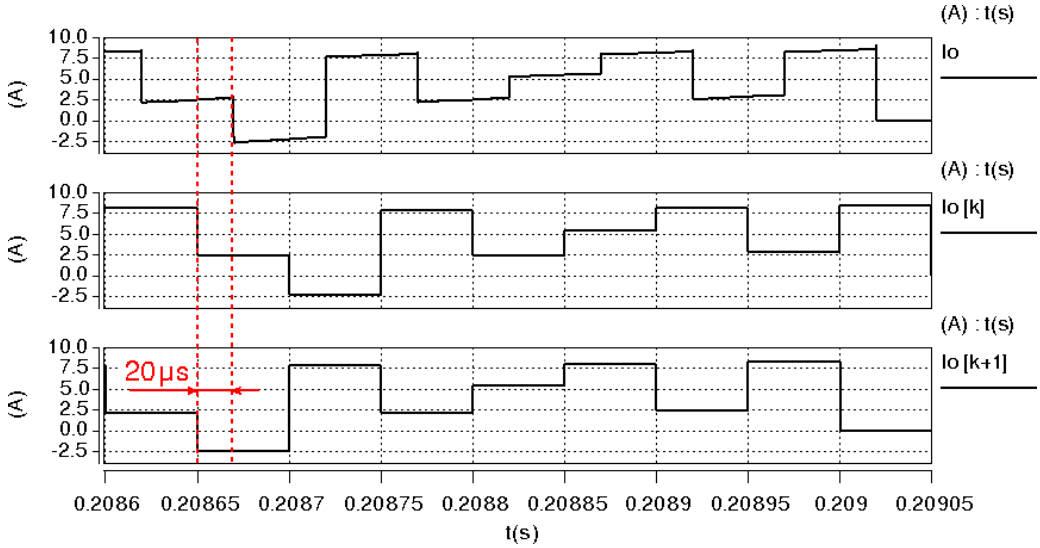

Fig. 4. Estimation of inverter input current I_O in steady-state

4. Digital implementation

Control implementation of the PQRDCLI in a parallel processing system comprises the TMS320C6711 floating point DSP Starter Kit (DSK) of Texas Instruments and the ACEX 1K Programmable Logic Device (PLD) of Altera. Management of tasks has been particularly described in [14]. The DSK realizes:

- u/f control of IM including generation of three-phase sinusoidal voltages reference for SDM,
- computation of subperiods $t_{1(ON)}$ and $t_{TF(ON)}$ for successive quasi-resonant cycle,

while the PLD performs:

- control of analog-to-digital four channels converter AD7864 for acquisition of IM currents i_A, i_B and input voltages U_{C2}, U_{DC}
- communication between DSK and PLD by common RAM block,
- sigma-delta modulation
- quasi-resonant cycle state machine for subsequent execution of $A - I$ intervals,
- diagnostics of IGBT drivers

The PQRDCLI operation cycle is governed by the SDM sampling interrupts frequency 20 kHz. Execution times of selected main tasks are presented in Table 2.

Table 2
Execution times of parallel processing devices

DSK [μs]	PLD [μs]	Selected control tasks
14	–	IM control
–	10	PQR state machine
–	6	ADC
14	–	$t_{1(ON)}(k+1)$ & $t_{TF(ON)}(k+1)$

5. Experimental results

Laboratory setup consists of power supply units PSU1, PSU2 regulating voltages of two serially connected capacitors $C_1 - C_2$ (Fig. 5). The PQRDCLI system feeds an induction motor (IM) of the 7.5 kW at no-load conditions. Voltage and current measurements were recorded using a Tektronix DPO4034 oscilloscope equipped with voltage P6139A and current TCP0030 probes. Common mode component of three-phase IM currents was measured by the Schaffner SMZ11 probe. In order to compare performance of the PQRDCLI in relation to the hard-switching inverter, a bypass switch was applied to the parallel quasi-resonant circuit. By using such an arrangement, comparative tests of both converter topologies in the same environment conditions were effected.

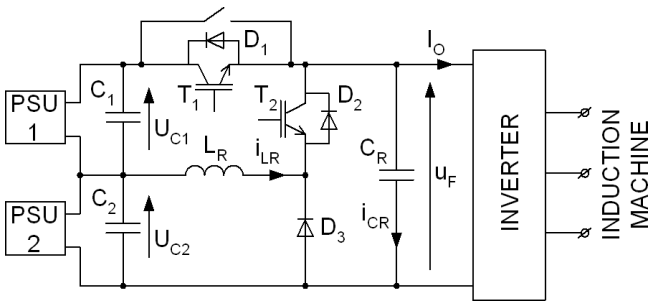

Fig. 5. Laboratory setup for experimental tests

Firstly, it has been confirmed quasi-resonant cycle operation in the parallel circuit $L_R - C_R$, as is depicted in Fig. 6. Without necessity of measuring the inductor current i_{LR}, precise timing of $t_{1(ON)}$ and $t_{F(ON)}$ periods assured approximately constant rate of change of the input inverter voltage $du_F/dt \approx \pm 100$ V/μs for rising and falling edge and independently of the IM phase current, (when the root mean square value changed from 2.2 A to 7.8 A). It is evident, that the same slopes characterize inverter output pulse voltages.

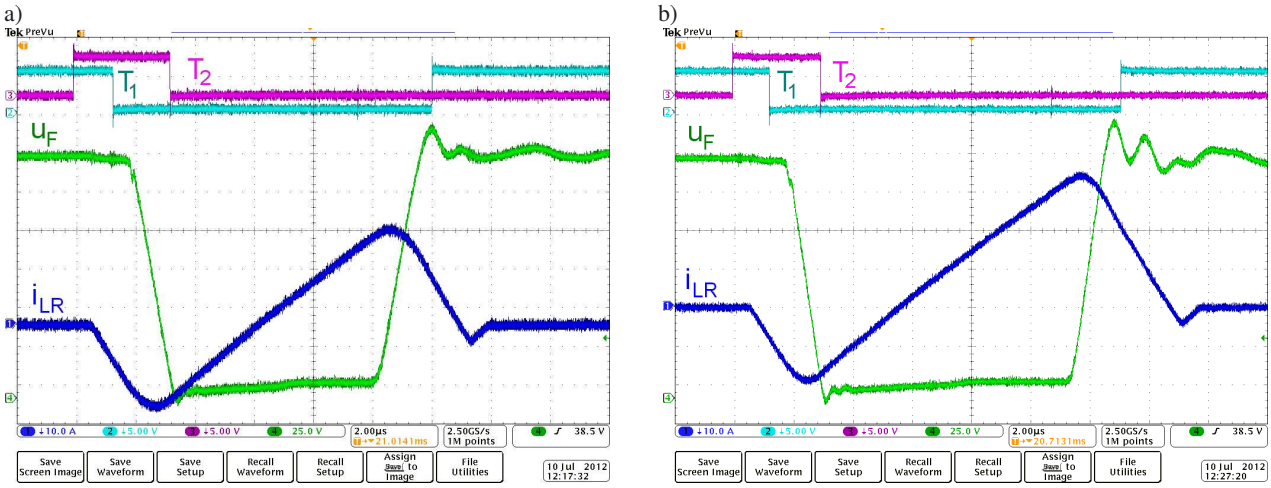

Fig. 6. Constant DC link voltage derivatives at variable load; a) $i_{A(rms)} = 2.2$ A, b) $i_{A(rms)} = 7.8$ A

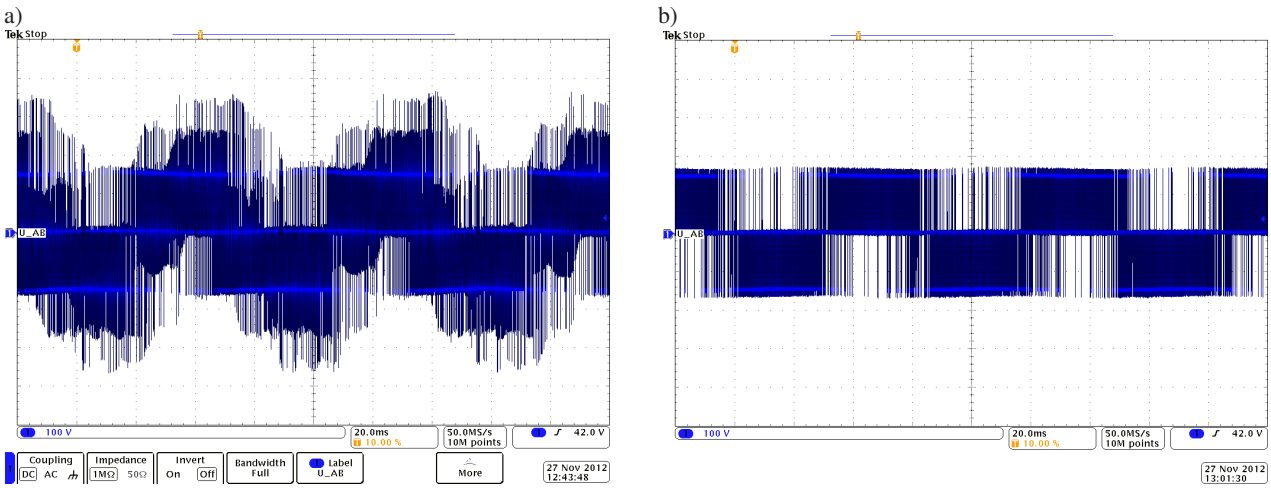

Fig. 7. Induction Motor line-to-line voltage; a) hard-switched inverter, b) PQRDCL inverter

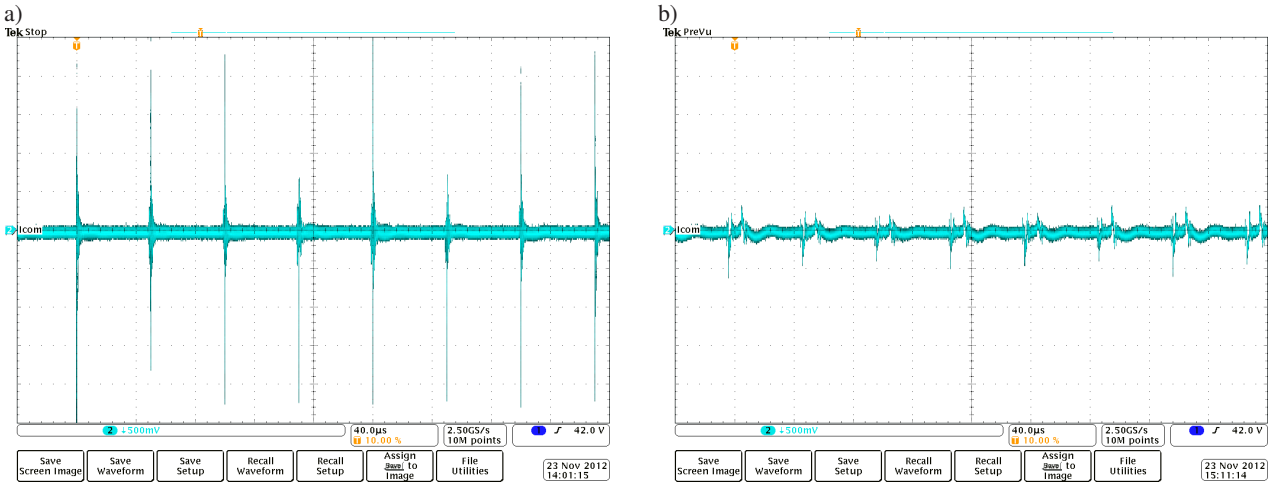

Fig. 8. Common mode component of induction motor currents (0.5A/div); a) hard-switched inverter, b) PQRDCL inverter

In the following Fig. 7 IM terminal line-to-line voltages of the PQRDCLI have been compared to the hard-switched inverter, when a bypass switch applied to the parallel quasi-resonant circuit was turned on. In the hard-switching inverter operation at pulse voltage derivatives of the order above ± 500 V/μs overvoltage spikes at motor terminals are evoked.

They are harmful for stator winding isolation durability, therefore hard-switched inverters usually require an auxiliary output filter. When operating with the PQRDCLI at significantly reduced line-to-line voltage rate of changes, overvoltage spikes at motor terminals have been eliminated.

In a third experiment depicted in Fig. 8, a common mode component of IM stator currents has been compared for two inverter arrangements. Again, in the case of high rate of voltage slopes of a hard-switching inverter, the every SDM cycle acting at sampling period $T_s = 50$ μs excites common mode current pulses with peak-to-peak amplitude of 4 A circulating through the parasitic IM capacitances. With reduced derivatives of the PQRDCLI voltage pulses and ZVS inverter operation, respective common mode current pulse peak-to-peak amplitudes have been attenuated to about 1 A.

6. Conclusions

In this paper, a novel predictive estimation based control strategy for a quasi-resonant dc link inverter feeding an induction motor drive is proposed. Due to resonant change of the dc link voltage and the ZVS operation of inverter switches, elimination of overvoltage spikes at motor terminals and the significant reduction of a common mode stator current component have been obtained. The considered method may be addressed to a border class of resonant and quasi-resonant dc link voltage inverters, whenever an input inverter current estimation is required for control algorithms.

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